What is claimed is:

1. An interleave address generation apparatus comprising:

interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses;

offset address generating means for generating offset addresses; and

adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses.

2. The interleave address generation apparatus according to claim 1, wherein the interleave address generating means comprising:

first variable converting means for converting a first variable using a predetermined first random pattern; and

second variable converting means for converting a second variable using a predetermined second random pattern, and

the offset address generating means uses a value obtained by multiplying said converted first variable by a maximum value of said second variable as an offset address.

3. The interleave address generation apparatus according

to claim 1, wherein the interleave address generating means comprising:

first variable converting means for converting a first variable using a predetermined random pattern; and

second variable converting means for converting a second variable based on said converted first variable, and

the offset address generating means uses a value obtained by multiplying said converted first variable by a maximum value of said second variable as an offset address.

4. The interleave address generation apparatus according to claim 3, wherein the interleave address generating means calculates an exclusive logical sum of a vector expression with a polynomial basis of a Galois field using the first variable converted by the first variable converting means as power in a power expression of the Galois field and a vector expression with a polynomial basis of the Galois field using the second variable converted by the second variable converting means as power in a power expression of the Galois field, and uses a result of converting the vector obtained to power in a power expression of the Galois field using a vector expression with a polynomial basis of the Galois field, as a converted second variable.

5. The interleave address generation apparatus according

to claim 1, wherein the offset address generating means outputs an offset address in accordance with the timing at which the interleave address generating means outputs an interleave address.

6. An interleave apparatus that comprises an interleave address generation apparatus and storing means for storing data, stores data in said data storing means in the sequence of addresses output from said interleave address generation apparatus and extracts data from said data storing means sequentially starting from the start address after a predetermined unit of data is stored, wherein said interleave address generation apparatus comprising:

interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses;

offset address generating means for generating offset addresses; and

adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses.

7. An interleave apparatus that comprises an interleave address generation apparatus and storing means for storing data, stores data in said data storing means sequentially starting from the start address and extracts data from said data storing means in the

sequence of addresses output from said interleave address generation apparatus after a predetermined unit of data is stored, wherein said interleave address generation apparatus comprising:

interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses;

offset address generating means for generating offset addresses; and

adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses.

8. A turbo coding apparatus comprising:

recursive convolutional coding means for carrying out convolutional coding of an information series; and

an interleave apparatus for carrying out interleave processing of said information series, wherein said interleave apparatus comprises interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses, offset address generating means for generating offset addresses, adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses and storing means for storing data, and extracts data from said data storing means sequentially starting from the start address after a predetermined unit of data is

stored.

9. A turbo decoding apparatus comprising:

soft decision output decoding means for decoding a code series;

a first interleave apparatus that carries out interleave processing on the output of this soft decision output decoding means;

soft decision output decoding means for decoding the code series whose input data sequence is rearranged by said first interleave apparatus; and

a second interleave apparatus that carries out deinterleave processing on the output of this soft decision output decoding means, wherein said first interleave apparatus and said second interleave apparatus comprise interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses, offset address generating means for generating offset addresses, adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses and storing means for storing data, store data in said data storing means in the sequence of interleave addresses output from said adding means and extract data from said data storing means sequentially starting from the start address after a predetermined unit of data is stored.

10. A communication terminal apparatus comprising an interleave apparatus and radio communication means for transmitting a signal output from said interleave apparatus or outputting the received signal to said interleave apparatus, wherein said interleave apparatus comprises interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses, offset address generating means for generating offset addresses, adding means for adding said offset addresses to said interleave addresses and outputting as interleave addresses and storing means for storing data, and stores data in said data storing means in the sequence of interleave addresses output from said adding means, and extracts data from said data storing means sequentially starting from the start address after a predetermined unit of data is stored.

11. A base station apparatus comprising an interleave apparatus and radio communication means for transmitting a signal output from said interleave apparatus or outputting the received signal to said interleave apparatus, wherein said interleave apparatus comprises interleave address generating means for generating an interleave address pattern of a predetermined size and sequentially outputting interleave addresses, offset address generating means for generating offset addresses, adding means for adding said offset addresses to said

interleave addresses and outputting as interleave addresses and storing means for storing data, and stores data in said data storing means in the sequence of interleave addresses output from said adding means, and extracts data from said data storing means sequentially starting from the start address after a predetermined unit of data is stored.

12. An interleave address generation method comprising the steps of:

converting a first variable using a predetermined random pattern;

converting a second variable using a predetermined random pattern; and

adding a result of multiplying said first variable by a maximum value of said second variable to said second variable.

13. An interleave address generation method comprising the steps of:

rearranging a first variable using a predetermined random pattern;

rearranging a second variable based on said rearranged first variable;

calculating an exclusive logical sum of a vector expression with a polynomial basis of a Galois field using said converted first variable as power in a power expression of the Galois field and a vector expression

with a polynomial basis of the Galois field using said converted second variable as power in a power expression of the Galois field;

converting the vector obtained to power in a power expression of the Galois field using a polynomial basis of the Galois field; and

adding a result of multiplying the conversion result by a maximum value of said first variable and said second variable to the conversion result.